LABORATORY 5

BASIC DIGITAL LOGIC CIRCUITS

OBJECTIVES

1. To study the characteristics of basic digital gates (NAND and NOR).
2. To use the logic gates to build simple logic circuits.

INFORMATION

Note: *Actual lab procedure follows this information section.*

1. Guidelines for building logic circuits

Throughout these experiments we will use CMOS chips to build circuits. The steps for wiring a circuit should be completed in the order described below:

- **MAKE SURE THE POWER IS OFF BEFORE YOU BUILD ANYTHING!**
- Plug the chips you will be using into the breadboard. Point all the chips in the same direction with pin 1 in the upper-left corner. (Pin 1 is often identified by a dot or a notch next to it on the chip package.)
- Build the circuit neatly. It will be easier to troubleshoot the circuits if they are neatly built.
- Connect +5V and GND pins of **each** chip to the power and ground bus strips on top of the PROTO-BOARD.
- Select a connection on your schematic and place a piece of hook-up wire between corresponding pins of the chips on your breadboard. It is better to make the short connections before the longer ones. Mark each connection on your schematic as you go, so you do not attempt to make the same connection again at a later stage.
- Get your TA to check the connections, before you turn the power on.
- If an error is made and is not spotted before you turn the power on. Turn the power off immediately before you begin to rewire the circuit.
- Tidy the area that you were working in and leave it in the same condition as it was before you started.

Common Causes of Problems

- Not connecting the ground and/or power pins for all chips.
- Leaving out wires.
- Plugging wires into the wrong holes.
- Driving a single gate input with the outputs of two or more gates
- Modifying the circuit with the power on.

If you damage a chip, inform your TA. He or she will get you a replacement chip. Don't put the faulty chip back in your kit or with other chips in the lab: Chips are inexpensive so it is best to discard chips that may cause problems.

Example Implementation of a Logic Circuit:

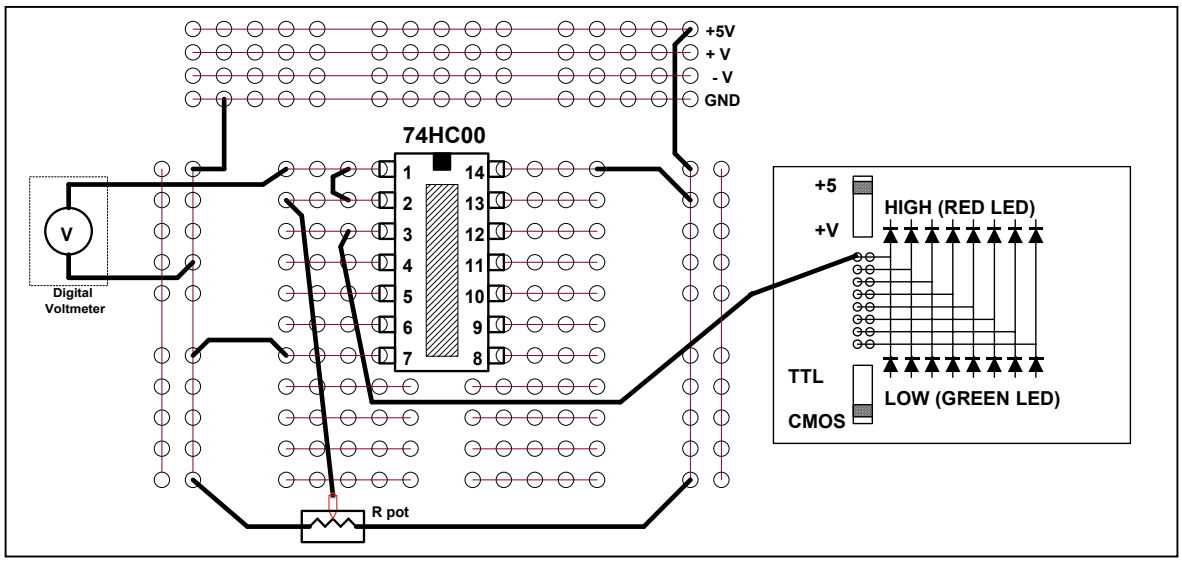


Figure 5.1 *A completely designed and connected circuit.*

2. IC technology introduction

The fabrication of common integrated circuits is based on the structuring of N-type and P-type semiconductors with a conducting material, sometimes aluminum, and an insulating silicon material. The manner in which these materials are put together determines the characteristics and function of the IC's. One of the characteristics dependent on the manner in which these materials are put together is the type of transistor used on the IC. Bipolar or conventional transistors are used in manufacturing *TTL* (transistor-transistor logic) devices. Field effect transistors or unipolar transistors are used to manufacture *PMOS* (P-type metal-oxide semiconductor), *NMOS* (N-type metal-oxide semiconductor) and *CMOS* (complementary metal-oxide semiconductor) devices. Each of these logic families, TTL, PMOS, NMOS and CMOS, has a specific set of characteristics that make it desirable for certain applications.

The TTL family's characteristics have made it the most popular logic family in industry. Although it does not stand out in any one area, its speed and reliability have made it popular.

CMOS is becoming increasingly popular. Its low power consumption and high fan-out make it a desirable choice when designing a circuit. CMOS's primary disadvantage is that it cannot be packed as densely as TTL or NMOS. This is due to the fact that each transistor in a CMOS circuit is actually made from a PMOS transistor and an NMOS transistor.

3. CMOS gate logical levels

In digital circuitry a circuit which recognizes a high level to be a logical-1 (true) and a low level as a logical-0 (false) is said to use *positive logic.* A circuit which uses a low level to represent logical-1 and a high level to represent logical-0 is said to use *negative logic.* Within each family there is a range of voltages that the circuit will recognize as a high or low level. Table 5.1 lists the ranges for high and low level voltages for TTL and CMOS IC families.

IC Logic Family	Voltage Supply (V)	High-Level Range (V)	Typical Voltage (V)	Low-level Range(V)	Typical Voltage (V)
Standard TTL	Vcc=5	2.4 to 5	3.0	0 to 0.4	0.2
CMOS	Vdd=3-15	Vdd	Vdd	0 to 0.5	0
Positive Logic			logic-1		logic-0

Table 5.1 *TTL and CMOS logical level voltages*

Typical input and output High and Low signal level thresholds of the CMOS gates powered by Vdd=5V are shown in Figures 5.2 and 5.3. As you can see, the input level thresholds are much wider than the output level thresholds, which allow design of complicated noise-proof IC circuits.

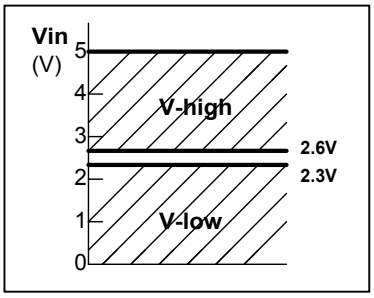


Figure 5.2 Typical input levels

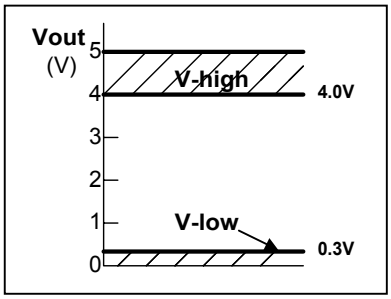


Figure 5.3 Typical output levels

4. Logic level indicators

There are digital logic level indicators built on the right side of your Proto-Board as shown in Figure 5.4. There are eight independently operating channels that are able to show the logic levels of digital signals connected to them. Each channel has two indicating LEDs. The Red LED will light up when the output voltage of the measured circuit is sufficiently high and it could be considered as a logic level of "1". The green LED will light up when the output voltage of the measured circuit voltage is sufficiently low and it could be considered as a logic level of "0".
There are two switches assigned to the logic indicator. One is to change the power supply of the indicator from +5(V) to +V(V) depending of what power supply source is connected to your circuit. The second switch position determines what kind of digital logic levels are supplied to the indicator. If the tested circuit is built using TTL ICs, the switch should be in the "TTL" position. If the tested circuit is built using CMOS ICs, the switch should be in the "CMOS" position. During the experiments, it is necessary to turn switch 1 to the "+5 V" position and switch 2 to the "CMOS" position.

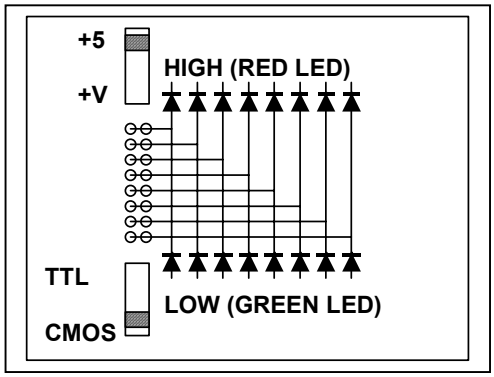


Figure 5.4 *Logic Level Indicators on Proto-Board*

5. Logic switches

There are eight digital logic switches (SW1 to SW8) built on the bottom left of your Proto-Board as shown in Figure 5.5 and each one is able to apply logic levels of 0 and 1 to the connected digital circuits. Another switch is assigned to change the voltage levels of the logic signals from +5(V) to +V(V) depending on what power supply source is connected to your circuit. During the experiments, it is necessary to turn the switch to the "+5 V" position.

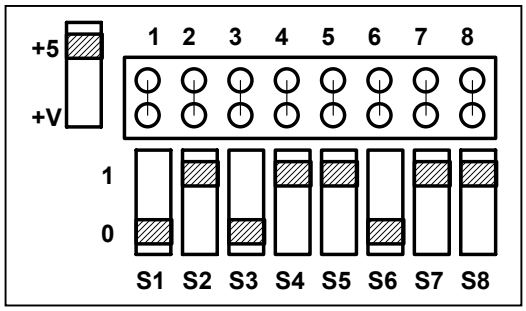


Figure 5.5 *Logic Switches on Proto-Board*

EQUIPMENT

1. Digital multimeter (Fluke 8010A, BK PRECISION 2831B or BK PRECISION 2831C)
2. PROTO-BOARD PB-503 (breadboard)
3. 2 x IC 74HC00, IC 74HC02
4. Capacitors 100nF, 47uF
5. Resistor 100kΩ

PRE-LABORATORY PREPARATION

The lab preparation must be completed before coming to the lab. Show it to your TA at the beginning of the lab and get his/her signature in the Signature section of the Lab Measurements Sheet.

This laboratory experiment uses the "black box" idea. It is not important, to begin with, that a student know how a particular IC functions electrically. It is more important that a student know what its function is and how it can be used within a larger circuit. As the following experiments are done, the emphasis will remain on using IC's to construct larger digital circuits.

There are several tasks that you must perform prior to this laboratory:

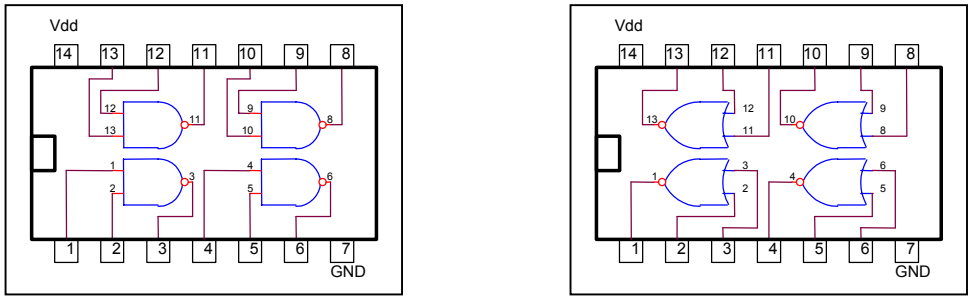
- Read the laboratory assignment in full.
- **[1 MARKS]** Draw the truth table of a 2-input NAND gate in Table 5.4 (section 1.2.1 of the Lab Measurements Sheet).
- **[1 MARKS]** Draw the truth table of a 2-input NOR gate in Table 5.5 (section 2.1 of the Lab Measurements Sheet).
- **[12 MARKS]** Design a 4-input NAND circuit using 2-input NAND gates in section 3.1 of the Lab Measurements Sheet. You will be granted full marks for the optimum design, which uses the minimum number of NAND gates.

- **[10 MARKS]** Draw the component connections of this circuit in section 3.2 of the Lab Measurements Sheet.
- **[1 MARKS]** Draw the truth table of a 4-input NAND circuit in Table 5.6 (section 3.3 of the Lab Measurements Sheet).
- **[15 MARKS]** Using only 2-input NAND gates design a circuit to realize truth Table 5.2. Draw the circuit diagram and the component connections of this circuit in sections 4.1 and 4.2 of the Lab Measurements Sheet. You will be granted full marks for the optimum design, which uses the minimum number of NAND gates.

Input A	Input B	Input C	Output Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Table 5.2 *Truth table for complex logic design.*

Chip Diagrams:



(a) *74HC00 (NAND)* **(b)** *74HC02 (NOR)*

Figure 5.6 *Chip diagrams*

PROCEDURE

1. The NAND Gate

1.1 Logic level measurements

The goal of this experiment is to determine the input and output logic level thresholds of the 74HCxx CMOS logic gates, powered by Vdd=+5V. To achieve this goal you will use 2-input NAND gate 74HC00 in the "inverter" connection, where two inputs are connected together

1.1.1. Connect the 2-input NAND gate as shown in Figure 5.7. Remember to power the Vdd to pin 14 and GND to pin 7 of the chip. For the power supply, use the built-in source of Vdd=+5V of your PROTO-BOARD (the top horizontal strip on the power bar). Remember also to leave the Power Supply turned off, until you are sure that your circuit is wired correctly. To achieve better circuit stability, connect capacitor C1 between Vdd and Ground close to pin 14 of the IC 74HC00. **Note:** Figure 5.1 shows how the circuit of Figure 5.7 should be wired.

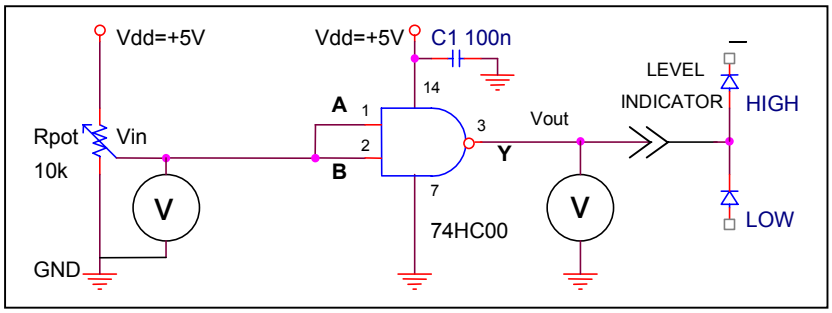


Figure 5.7 *NAND gate threshold test circuit.*

1.1.2. Using the same source of Vdd = +5V and a built-in potentiometer Rpot = 10kΩ at the bottom of your PROTO-BOARD, create a variable voltage **Vin** to provide input signal to the inputs of the NAND gate.

When the layout has been completed, have your TA check your breadboard for errors and ***get his/her signature in the Signature section of the Lab Measurements Sheet. You will be penalized marks if your sheet is not initialed.***

1.1.3. Starting from 0V turn the potentiometer and slowly increase the input voltage. Measure the voltage applied to the inputs using a Digital Voltmeter. Determine what is the input voltage range Vin-min(V) and Vin-max(V) for which the output Y is in the "HIGH" state (i.e., the RED LED is ON). Put the values in Table 5.3 in section 1.1 of your Lab Measurements Sheet.

1.1.4. Keep increasing Vin up to +5V. Determine what is the input voltage range Vin-min (V) and Vin-max(V) for which the output Y is in the "LOW" state (i.e., the GREEN LED is ON). Put the values in Table 5.3 in section 1.1 of your Lab Measurements Sheet.

1.1.5. Connect the Digital Voltmeter to the output Y. Sweep the input voltage from 0V to +5V. What is the output voltage range Vout-min and Vout-max for which the logic indicator shows levels of 1 and 0? Record the values in Table 5.3 in section 1.1 of your Lab Measurements Sheet.

1.1.6. Draw the input and output voltage ranges in the diagrams in Figure 5.10 and Figure 5.11 in section 1.2 of your Lab Measurements Sheet. What are your conclusions about the input threshold and output logic level voltage properties of the 74HCxx NAND gates powered by Vdd=+5V? Answer the question in section 1.3 of the Lab Measurements Sheet.

1.2. The NAND gate truth table

1.2.1. Connect the 2-input NAND gate (74HC00) as shown in Figure 5.8. Remember to leave the Power Supply turned off, until you are sure that your circuit is wired correctly. Connect the Y (output) of the gate to the Logic Level Indicator. Attach the input A to the connector of LOGIC SWITCH S1 and input B to the connector of LOGIC SWITCH S2 at the bottom left of your PROTO-BOARD. To achieve better circuit stability, connect capacitor C1 between Vdd and Ground close to pin 14 of the IC 74HC00.

When the layout has been completed, have your TA check your breadboard for errors and ***get his/her signature in the Signature section of the Lab Measurements Sheet. You will be penalized marks if your sheet is not initialed.***

1.2.2. Vary the inputs A and B (i.e., 0 and 1) to obtain all the possible combinations and complete the truth table for the NAND gate. Give the values for the truth table in Table

5.4 in section 1.2.1 of the Lab Measurements Sheet. Compare the results with your pre-lab.

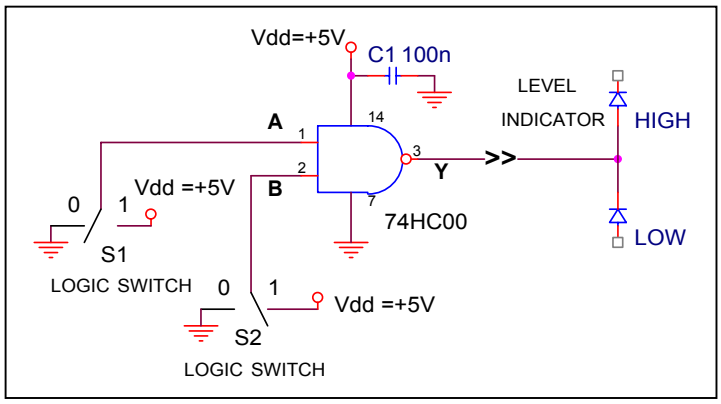


Figure 5.8 *The 2-input NAND gate.*

WARNING: To prevent damage of the circuits turn the **"+5V/ +V"** switch in the LOGIC SWITCHES area to the **"+5V"**position before applying power to the circuit.

2. The NOR gate

2.1. Connect the 2-input NOR gate (74HC02) as shown in Figure 5.9. Remember to leave the Power Supply turned off, until you are sure that your circuit is wired correctly. Connect the Y (output) of the gate to the Logic Level Indicator. Connect the input A to the LOGIC SWITCH S1 and input B to the LOGIC SWITCH S2 of your PROTO-BOARD.

WARNING: 1. Make sure your circuit is connected properly. The chip diagram of the 74HC02 is different from the chip diagram of 74HC00.

2. To achieve better circuit stability, connect capacitor C1 between Vdd and Ground close to pin 14 of the 74HC02.

2. To prevent damage to the circuits, turn the "+5V/ +V" switch in the LOGIC SWITCHES area to the "+5V"position before applying power to the circuit.

When the layout has been completed, have your TA check your breadboard for errors and ***get his/her signature in the Signature section of the Lab Measurements Sheet. You will be penalized marks if your sheet is not initialed.***

2.2. Vary the inputs A and B (i.e., 0 and 1) to obtain all the possible combinations and complete the Truth table for the NOR gate. Give the values for the truth table in Table 5.5 in section 2.1 of the Lab Measurements Sheet. Compare the results with your pre-lab.

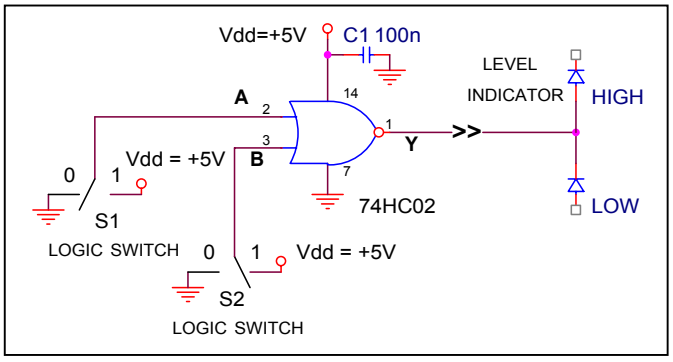


Figure 5.9 *The 2-input NOR gate.*

3. The 4-input NAND gate

3.1 Build the circuit that you designed in sections 3.1 and 3.2 of the Lab Measurements Sheet on your PROTO-BOARD. Use the LOGIC SWITCHES S1 to S4 to provide input signals to your circuit.

When the layout has been completed, have your TA check your breadboard for errors and ***get his/her signature in the Signature section of the Lab Measurements Sheet. You will be penalized marks if your sheet is not initialed.***

3.2 Use the LOGIC SWITCHES S1 to S4 to provide input signals to your circuit. Vary the inputs A, B, C and D (i.e., 0 and 1) to obtain all the possible combinations and complete the truth Table 5.6 in section 3.3 of the Lab Measurements Sheet.

3.3 Compare the measured truth table 5.6 of this circuit with your pre-lab truth table in section 3.4 of the Lab Measurements Sheet.

4. Complex logic

4.1. Build the circuit that you designed in sections 4.1 and 4.2 of the Lab Measurements Sheet on your PROTO-BOARD. Use the LOGIC SWITCHES S1 to S3 to provide input signals to your circuit.

When the layout has been completed, have your TA check your breadboard for errors and ***get his/her signature in the Signature section of the Lab Measurements Sheet. You will be penalized marks if your sheet is not initialed.***

4.2. Vary the inputs A, B and C (i.e., 0 and 1) to obtain all the possible combinations and complete the truth Table 5.7 in section 4.3 of the Lab Measurements Sheet.

4.3. Compare the measured truth table 5.7 of this circuit with your pre-lab assignment truth table in section 4.4 of the Lab Measurements Sheet.

5. OPTIONAL

Digital integrated logic circuits can also be used in several unusual applications. Figure 5.10 shows a square waveform generator built on two NAND gates.

5.1. Connect the circuit on the breadboard and show it to your TA.

5.2. Observe the output waveform and explain how this circuit operates. How does the output signal change when you change the potentiometer position and its resistance?

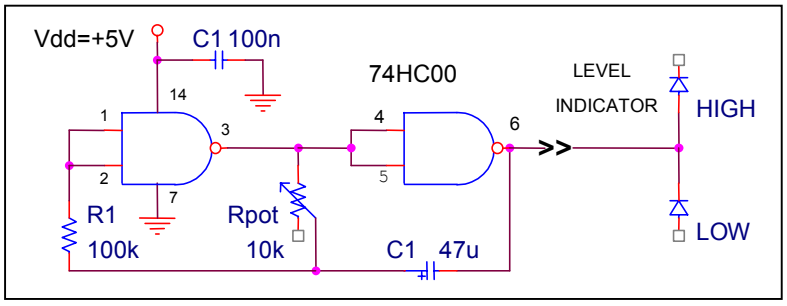


Figure 5.10. Two *NAND gates generator circuit*

LAB MEASUREMENTS SHEET – LAB 5

Name _____

Student No_____

Workbench No_____

NOTE: Questions are related to observations, and must be answered as a part of the procedure of this experiment.

Sections marked * are pre-lab preparation and must be completed BEFORE coming to the lab.

1. NAND gate

1.1. **Table 5.3** *Input and output logic level voltages for a 2-input NAND gate*

Input			**Output**		
Input Logical level	Vin-min (V)	Vin-max (V)	Output Logical level	Vout-min (V)	Vout-max (V)
0			1		
1			0		

1.2. Input and output logical level thresholds for the 2-input NAND gate

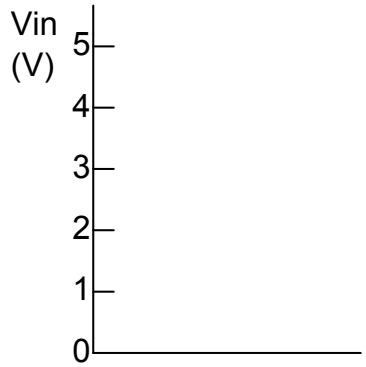


Figure 5.10 *Input levels*

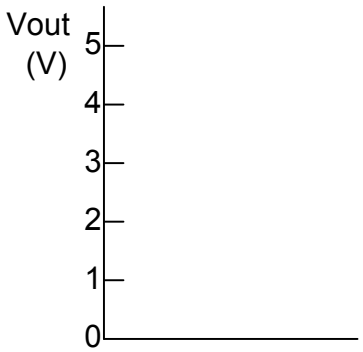


Figure 5.11 *Output levels*

1.3. What are your conclusions about the threshold and output logic level voltage properties of the 74HCxx NAND gates powered by Vcc=+5V?

_____

_____

_____

_____

_____

_____

1.2. The NAND gate truth table

1.2.1. Draw the truth table of a 2-input NAND gate.

Table 5.4 *Truth table for the 2-input NAND gate*.

Input A	Input B	Output Y* (Prelab)	Output Y (Measured)
0	0		
0	1		
1	0		
1	1		

1.2.2. Compare the pre-lab and measured output levels for Table 5.4.

2. The NOR gate truth table

2.1. Draw the truth table of 2-input NOR gate.

Table 5.5 *Truth table for the 2-input NOR gate*.

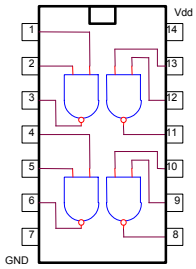
Input A	Input B	Output Y* (Prelab)	Output Y (Measured)
0	0		
0	1		
1	0		
1	1		

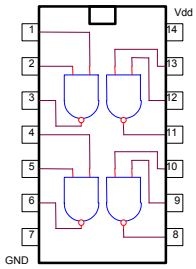
2.2. Compare the pre-lab and measured output levels for Table 5.5.

3. The 4-input NAND gate

*3.1. Design 4-input NAND circuit using 2-input NAND gates and draw the circuit diagram in the space below (Prelab).

*3.2. Draw the component connections of this circuit using 74HC00 diagrams below (Prelab).





*3.3. Draw the truth table of 4-input NAND gate.

Table 5.6 *Truth table for 4-input NAND gate*

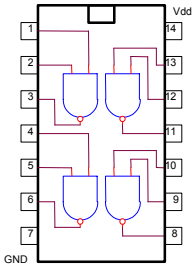
Input A	**Input B**	**Input C**	**Input D**	**Output Y* (Prelab)**	**Output Y (Measured)**
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

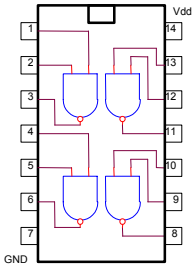
3.4. Compare the pre-lab and measured output levels for Table 5.6.

4. Complex logic

* 4.1. Using only 2-input NAND gates realize the truth table 5.2 and draw the circuit diagram in the space below (Prelab).

* 4.2. Draw the component connections of the circuit designed in section 4.1 using the 74HC00 diagrams below (Prelab).





4.3. Draw the truth table for the circuit, designed in sections 4.1 and 4.2.

Table 5.7 *Truth table for complex logic design.*

Input A	Input B	Input C	Output Y	Output Y (Measured)
0	0	0	0	
0	0	1	0	
0	1	0	1	
0	1	1	1	
1	0	0	0	
1	0	1	0	
1	1	0	1	
1	1	1	0	

4.4. Compare the truth table of this circuit with the truth table 5.2.

_____

_____

5. OPTIONAL. Explain how the circuit in Figure 5.10 operates. How the output signal is changing when you change the potentiometer position and its resistance?

_____

_____

_____

_____

_____

_____

SIGNATURES **TA NAME:_____**

To be completed by TA during the lab session.

Check Boxes						TA Signature	Student's Task
							Pre-lab completed.
							Circuit of Figure 5.7 connected and equipment used correctly
							Circuit of Figure 5.8 connected and equipment used correctly
							Circuit of Figure 5.9 connected and equipment used correctly
							4-input NAND connected and equipment used correctly
							Design circuit connected and equipment used correctly
							Data collected and observations made

MARKS

To be completed by TA after the lab session.

Granted Marks	Max. Marks	Student's Task
	40	Pre-lab preparation
	10	Circuit of Figure 5.7 connected and equipment used correctly
	10	Circuit of Figure 5.8 connected and equipment used correctly
	10	Circuit of Figure 5.9 connected and equipment used correctly
	10	4-input NAND connected and equipment used correctly
	10	Design circuit connected and equipment used correctly
	10	Data collected and observations made
	100	**Total**